High-Gain, Low-Voltage Operational Amplifier with 18nm FinFET Technology for Application in ADCs

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***Abstract*—This paper proposes an operational amplifier (OpAmp) architecture designed to operate at low voltage while achieving high gain. Utilizing 18 nm FinFET technology, the proposed OpAmp targets applications in analog-to-digital converters (ADCs). The design employs a two-stage, the input stage has an operational transconductance amplifier (OTA) folded-cascode topology with use of composite cascode to reach high gain. Key specifications include a supply voltage of 700 mV, power dissipation of less than 10 µW, and a minimum slew rate of 10 V/µs. Simulation results confirm the OpAmp's robust performance, with a DC Gain of 79.16 dB, Power Comsumption of 5.04 µW, Unity Gain Band-Width (UGBW) of 42.29 MHz, slew rate of 22.66 V/µs, Phase Margim of 52.68° and CMRR of 87.57 dB.**

***Index Terms*—Operational transcondutance amplifier, Low voltage, High gain, FinFET, Folded cascode, Composite cascode.**

I. Introduction

The demand for nanoscale integrated circuits has significantly increased in recent years, driven by the growing need for low-power designs, particularly in portable systems [1]. These low-power circuits rely on both reduced component dimensions and supply voltage to achieve power efficiency. However, as dimensions continue to shrink, designers must consider effects like channel length modulation [2], which cannot be neglected.

Consequently, conducting comprehensive studies that aim to make circuits more efficient is essential, focusing on high DC gain, low power, low voltage, and wide unity gain bandwidth (UGBW). Operational amplifiers (op-amps) with these attributes have significant relevance in applications, such as A/D converters, signal sampling circuits, medical devices, and biosensors [3].

Reducing power consumption while maintaining high gain and a high UGBW in op-amps can be achieved by decreasing the channel length. By doing so, lowering the power supply can reduce thermal losses, thus achieving more efficient power efficiency. However, achieving low power losses and high gain simultaneously is challenging, primarily due to the effects of channel length reduction [4]. To mitigate these effects, new transistors geometries, such as the FinFET (Fin Field Effect Transistor), have been explored [5]. FinFET transistors favor the implementation of such circuits, offering advantages like improved gate voltage control and reduced channel modulation effect, thus providing better analog characteristics compared to planar FETs .

Stability is a vital aspect of op-amp performance. Op-amp systems can be made more stable by employing compensation techniques. It can be used to create faster, lower-power op-amps with better power supply noise rejection (PSRR) in both two-stage and multistage op-amps. Additionally, cascode compensation can be utilized to further increase stability, particularly when driving high capacitive loads [4].

Beyond process parameter solutions, geometric optimizations, and the analog characteristics of the operational amplifier, it is crucial to select an architecture that meets the necessary project demands: high gain and high UGBW. With that in mind, using a fully differential folded-cascode op-amp is a good choice [6]. For an additional increase in gain, employing two fully differential folded-cascode op-amps can be beneficial. The use of this architecture brings several advantages, one of which influences the size of the layout, as the composite cascode op-amp allows for a smaller cell size. This enables the reduction of the compensation capacitor, as well as supports low power supply for the drain current [1].

In this work, an op-amp architecture using a two-stage folded-cascode topology is proposed to increase the DC gain, utilizing indirect compensation techniques to achieve a higher unity gain-bandwidth and greater stability for capacitive loads. For this, the g_m/I_D methodology was used for sizing the components that make up the desired circuit. Based on the project, simulations were carried out using the Cadence Virtuoso ADE Suite, with 18nm using the Advanced Nodes GPDK supplied by Cadence Design Systems. The results were analyzed and discussed.

This paper is organized as follows: The principles and benefits of applying the folded-cascode technique are presented in Section II. The basic concepts of indirect compensation for op-amps are covered in Section III. Section IV presents the methodology g_m/I_D for the design of the proposed architecture. Section V showcases the design of the proposed architecture,the simulated circuit and the results. The conclusions are given in Section VI.

II. Composite Cascode Amplifier

The composite cascode techniques are commonly employed to gain specific advantages, particularly in terms of gain, bandwidth, and high-frequency performance.

The classic cascode amplifier configuration is comprised of two transistors combined, where one operates as an amplifier and the other as a load, as shown in Fig. 1(a). In the composite cascode amplifier the load transistor is connected in a way that the input signal is applied to the gate terminal of both transistors, as observed in Fig. 1(b).

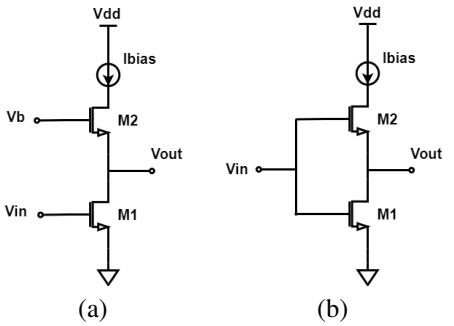

Fig. 1. (a) Conventional cascode amplifier (b) Composite cascode amplifier.

The use of the composite cascode technique is advantageous because it maintains the high voltage gain characteristic of cascode amplifiers, reduces the effects of Miller capacitance, increases the amplifier's bandwidth, and offers good performance in a relatively small space [7].

The voltage gain magnitude Av_{01} for the topology presented in Fig. 1(a), can be represented by:

$$|Av_{01}| = g_{m1}r_{o1} + g_{m1}r_{o1}(g_{m2} + g_{mb2})r_{o2}. \quad (1)$$

For Fig. 1(b), Av_{02} can be written as

$$|Av_{02}| = g_{m1}r_{o1} + g_{m2}r_{o2} + g_{m1}r_{o1}(g_{m2} + g_{mb2})r_{o2}, \quad (2)$$

where r_{oi} is the output resistance of M_i, g_{mi} is the transconductance, and g_{mbi} is the body effect transconductance.

Evaluating Eqs. 1 and 2, it can be seen that the gain of the composite cascode topology is greater than that of the conventional topology.

III. The g_m/I_D methodology for analog design

The g_m/I_D technique is strategic in the design of operational amplifiers, as it relates transconductance per drain current, facilitating rapid and accurate performance assessment of circuits. This methodology allows for direct analyses based on the dimensions and intrinsic gain of the transistors, offering flexibility in transistor sizing and a clear view of how these choices impact circuit performance. Moreover, it adapts well to advanced semiconductor technologies, maintaining its effectiveness despite scaling challenges and process variations, which is crucial for optimizing circuit designs under modern manufacturing conditions [8].

This ratio (g_m/I_D) is significant because it is unaffected by the gate width of the transistor, meaning it is a useful constant for predicting transistor behavior regardless of its specific physical dimensions [9].

The drain current is a crucial factor in determining a circuit's capacity to reach maximum performance in terms of the frequency at which the circuit can operate before gain begins to decline. This drain current can be calculated by:

$$I_D = g_m/(g'_m/I_N) \quad (3)$$

with $I_N = I_D/W$. Here, g_m represents the transconductance of the device, while g'_m/I_N is a ratio that reflects the transistor's efficiency, calculated from a device whose width (W) and length (L) dimensions are known [8].

Knowing the drain current (I_D) enables the determination of W, using the following relationship:

$$W = I_D/I_N \quad (4)$$

After simulations of a single transistor, to describe its g_m/I_D, for N-type and P-type, the data is plotted in the g_m/I_D vs. V_{gs} curves, Fig. 2 and 3. These curves are separated for N-type and P-type transistors, providing a comparative analysis between these two categories. On the g_m/I_D curves, it can be observed that in strong inversion, the g_m/I_D ratio varies between 5 and 10. This range indicates that the transistors are operating with high efficiency and low output resistance, typical of operations where high gain is needed. In moderate inversion, the ratio increases to 10 to 20, reflecting an intermediate state where the transistor still maintains good efficiency, albeit with a lower gain compared to strong inversion. Finally, in weak inversion, the (g_m/I_D) ratio is greater than or equal to 20, indicating that the transistor operates with reduced efficiency and higher output resistance, which is characteristic of low power consumption conditions.

With the values obtained from the previous curves, it is necessary to evaluate the I_N vs. g_m/I_D curve, with g_m/I_D and I_D known it is simply a matter of evaluating the curve and determining the W parameter efficiently and practically.

IV. OpAmp Design

The proposed architecture of the operational amplifier can be seen in Figure 4. It consists of two stages: the input stage is a operational transconductance amplifier in composite and folded cascode (M1, M2, M3, and M4). The output stage (M13, M14, M15, and M16) is an amplifier to increase gain. The transistors M9, M10, M11, and M12 are designed using the composite cascode technique for biasing the input stage. A capacitor $Cc1$ is used for miller compensation.

The entire design of the operational amplifier was done in 18 nm FinFET technology, and the simulations were performed with the GPDK provided by Cadence Design Systems.

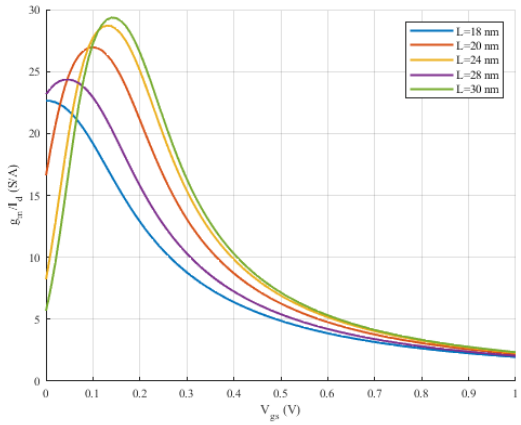

Fig. 2. FinFET characteristics curves g_m/I_D with W = 62 nm, N type

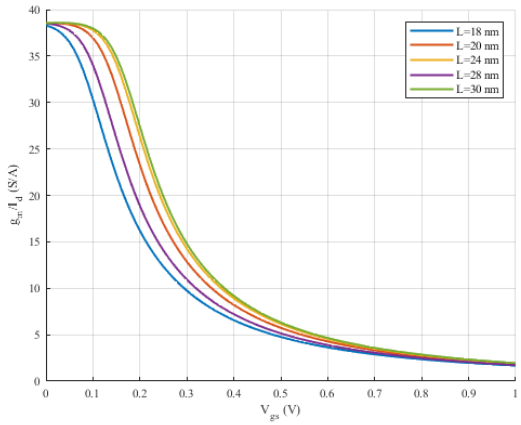

Fig. 3. FinFET characteristics curves g_m/I_D with W = 62 nm, P type

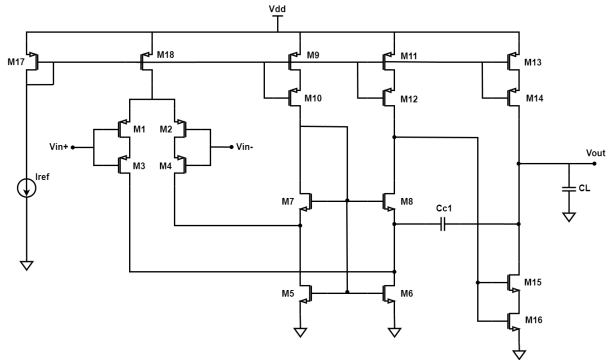

Fig. 4. Proposed architecture, op-amp with folded cascode technique.

A. Design of the First Stage

For transistors M1 and M2, it was necessary to make them operate in the subthreshold region with weak inversion ($gm/I_D = 28\,S/A$), because the efficiency of the transistor is higher to provide elevated gain, while transistors M3 and M4 operating in strong inversion region ($gm/I_D = 4\,S/A$). Another point to consider in sizing this stage is that the W/L ratio of M1 and M2 should be much smaller than that of M3 and M4.

B. Design of the Second Stage

For transistors M14 and M15, the W/L ratio should be sized so that they operate in the subthreshold region ($gm/I_D = 28\,S/A$), while transistors M13 and M16 should operate in the moderate or strong inversion region ($gm/I_D = 4\,S/A$). In this stage, the output resistance of transistors M14 and M15 contributes to a higher overall gain of the operational amplifier.

C. Specifications

The OpAmp design specifications are: $A_0 \geq 50dB$, $V_{DD} = 700mV$, $C_L = 100fF$, $SlewRate \geq 10V/\mu s$ (minimum slew rate), $I_{min} = SR \cdot CL \geq 1\mu A$, $UGBW \geq 50MHz$, $P_{diss} \leq 10\mu W$ (Maximum power dissipation), $I_{max} = P_{diss}/V_{DD} = 14.286\mu A$, $L = 30nm$. With those specifications, the width of transistors and the Miller compensation capacitor (Cc1) are listed in the Table I.

TABLE I
WIDTH OF TRANSISTORS (m) AND COMPENSATION CAPACITOR (F)

M1-M2	1.406 μ	**M14**	3.806 μ
M3-M4	3.806 μ	**M15**	1.406 μ
M5-M6	1.886 μ	**M16**	446 n
M7-M8	734 n	**M17**	1.886 μ
M9-M11	446 n	**M18**	1.406 μ
M10-M12	2.846 μ	**Cc1**	100 f
M13	446 n		

V. SIMULATION AND RESULTS

A. DC Gain, Phase Margin and Unity Gain-Bandwith

Simulations were performed for open-loop DC gain ($79.16dB$), phase margin ($52.68°$), and unity gain-bandwidth ($42.29MHz$). These results are shown in the Figure 5.

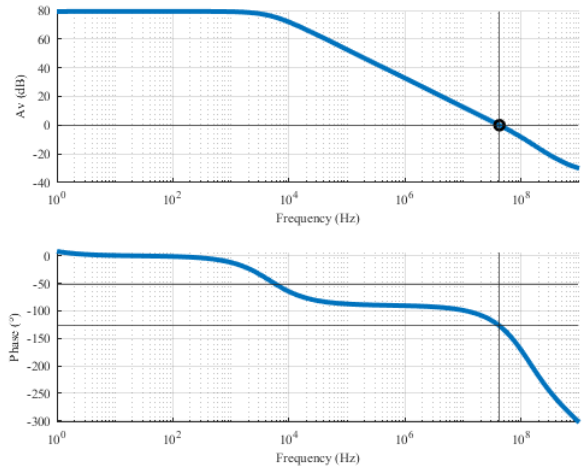

Fig. 5. Frquency Response for $C_L = 100$ fF

B. CMRR

The value of the CMRR can be obtained using Equation 5, where Av_{DM} is the differential gain and Av_{CM} is the common-mode gain. The result can be seen in Figure 6. A high CMRR means a low common-mode gain, which represents the good quality of an operational amplifier.

$$CMRR(dB) = 20 \cdot log(\frac{Av_{DM}}{Av_{CM}}) \tag{5}$$

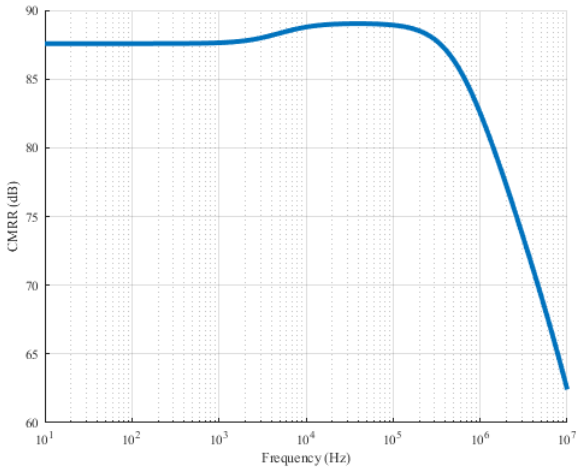

Fig. 6. CMRR result

C. Slew Rate

The Slew Rate is defined as the maximum rate of change of the output voltage and can be calculated using Equation 6, where Iss is the tail current of the amplifier and C_L is the load capacitance. The Slew Rate result was $22.66V/\mu s$.

$$SR = Iss/C_L \tag{6}$$

TABLE II
SIZE OF TRANSISTORS AND COMPENSATIONS CAPACITORS

Parameters	This work-FinFET	[1]-Planar	[10]-FinFET
$VDD(V)$	0.7	0.7	1.8
$Tech$	18 nm	0.18 μm	16 nm
$DCGain(dB)$	79.16	90.1	15.36
$UGBW$	42.29 MHz	309 kHz	5.07 GHz
$PM(degree)$	52.68	57.6	-
$CMRR(dB)$	87.57	100.3	76.67
SR	22.66 V/μs	65.52 V/ms	17.5 V/μ s
$Pdiss$	5.04 μW	891 nW	537.1 μ W
C_L	100 fF	15 pF	5 fF

The proposed operational amplifier architecture was designed to have high gain ($> 60dB$) and low supply voltage ($< 1V$) while maintaining a trade-off relationship with the slew rate. Using 18 nm FinFET technology, the circuit was simulated with Cadence's Virtuoso software. The advantages of the composite cascode can be evaluated from Table II. Compared to other architectures and technologies, it shows a good relationship between DC gain ($79.16dB$), supply voltage ($0.7V$), power dissipation ($5.04\mu W$), and Slew Rate ($22.66V/\mu s$).

To evaluate the design in comparison to other works, the Figure of Merit (FOM) for the proposed work was calculated and compared. The value obtained for the first Figure of Merit (FOM) [1], defined by Equation 7, in this work was $94.88 \cdot 10^{13}$. For [1], it was $4.46 \cdot 10^{13}$, and for [10], it was $8.05 \cdot 10^{13}$.

$$FOM_1 = (Gain \cdot UGBW)/(VDD \cdot Pdiss) \tag{7}$$

The value obtained for the second figure of merit, defined by Equation 8, in this work was $449.6 \cdot 10^{-3}$. For [1], it was $1103 \cdot 10^{-3}$, and for [10], it was $0.16 \cdot 10^{-3}$.

$$FOM_2 = (SR \cdot C_L)/(Pdiss) \tag{8}$$

It's possible to observe that although the FOM_2 in this study is lower than in [1], there is a considerable gain for the FOM_1. Since this work aims for the highest possible gain with the best relationship between supply voltage and power dissipation, the proposed architecture stands out compared to [1] and [10].

VI. CONCLUSION

In this paper, a high-gain operational amplifier architecture designed to operate at low voltage was proposed and subsequently verified through simulations. The gm/Id technique was used for the transistor sizing aimed at achieving high gain. Additionally, the use of the composite cascode topology proved efficient in terms of gain, although it exhibited a disadvantage regarding the unity-gain bandwidth. Compared to other works, a significant improvement in the Slew Rate was demonstrated, indicating that the amplifier proposed in this work can be employed in high-speed circuits, such as AD converters.

ACKNOWLEDGMENT

This work has been partially funded by the project "Research, experimentation, and evaluation of new hardware platforms, sensors, and intelligent sensing components" supported by the EMBRAPII VIRTUS COMPETENCE CENTER IN INTELLIGENT HARDWARE FOR INDUSTRY - VIRTUS-CC, with financial resources from the HardwareBR PPI of the MCTI grant number 055/2023, jointly with EMBRAPII.

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